AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-3 (Canceled).

4. (Original) An execution unit adapted to perform at least a portion of the Data Encryption Standard, the execution unit comprising:

a) a Left Half input;

b) a Key input;

c) a Table input;

d) a first group of transistors configured to receive the Table input, perform a table look-up, and output data;

e) a first exclusive-or operator having two inputs and an output, the first exclusive-or operator configured to receive the Left Half input and the Key input;

f) a second exclusive-or operator having two inputs and an output, the second exclusive-or operator configured to receive the data output by the first group of transistors and the output of the first exclusive-or operator; and

g) a third exclusive-or operator having two inputs and an output, the third exclusive-or operator configured to receive the Left Half input and the data output by the first group of transistors.

5. (Original) The execution unit of claim 4, further comprising a second group of transistors configured to receive data output by the second exclusive-or operator.

6. (Original) The execution unit of claim 4, wherein the execution unit is operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or an OFB mode of DES encryption at the same time that the first group of transistors performs one or more of the following actions: receiving the table input, performing the table look-up, and outputting data.

7. (Currently amended) An execution unit adapted to perform at least a portion of the Data Encryption Standard, the execution unit comprising:

a) a Left Half input;

b) a Key input;

c) a Table input;

d) a first group of transistors configured to receive the Table input, perform a table look-up, and output data;

e) a first exclusive-or operator having two inputs and an output, the first exclusive-or operator configured to receive the Left Half input and the Key input;

f) a second exclusive-or operator having two inputs and an output, the second exclusive-or operator configured to receive the output of the first group of transistors and the output of the first exclusive-or operator;

g) a third exclusive-or operator having two inputs and an output, the third exclusive-or operator configured to receive the Left Half input and the output of the first group of transistors and the output of the first exclusive-or operator; and

h) a multiplexer, the multiplexer having two data inputs and an output, the first of the two data inputs configured to receive the output of the first exclusive-or operator, the second of the two data inputs configured to receive the output of the second exclusive-or operator.

8. (Original) The execution unit of claim 7, further comprising a second group of transistors configured to receive data output by the multiplexer.

9. (Original) The execution unit of claim 7, wherein the execution unit is operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or an OFB mode of DES encryption at the same time that the first group of

transistors performs one or more of the following actions: receiving the table input, performing the table look-up, and outputting data.

10. (Currently amended) An execution unit adapted to perform at least a portion of the Data Encryption Standard, the execution unit comprising:

a) a Left Half input;

b) a Key input;

c) a Table input;

d) a Select input;

e) a first group of transistors configured to receive the Table input, perform a table look-up, and output data;

f) a first exclusive-or operator having two inputs and an output, the first exclusive-or operator configured to receive the Left Half input and the Key input;

g) an AND operator, the AND operator having two inputs and an output, the first of the two inputs of the AND operator configured to receive the output of the first group of transistors, the second of the two inputs of the AND operator configured to receive the Select input;

h) a second exclusive-or operator having two inputs and an output, the second exclusive-or operator configured to receive the output of the AND operator and the output of the first exclusive-or operator; and

i) a third exclusive-or operator having two inputs and an output, the third exclusive-or operator configured to receive the Left Half input and the output of the first group of transistors.

11. (Original) The execution unit of claim 10, further comprising a second group of transistors configured to receive data output by the second exclusive-or operator.

12. (Original) The execution unit of claim 10, wherein the execution unit is operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or an OFB mode of DES encryption at the same time that the first group of transistors performs one or more of the following actions: receiving the table input, performing the table look-up, and outputting data.

13-15 (Canceled).

16. (Currently amended) An execution unit adapted to perform at least a portion of the Data Encryption Standard, the execution unit comprising:

a) a Left Half input;

b) a Key input;

c) a Table input;

d) a Select input;

e) a first group of transistors configured to receive the Table input and the Select input, perform a table look-up, and output, via a first output, the result of the table look-up, the first group of transistors further configured to output the result of the table look-up, via a second output, if the Select input is a first value, and configured to output a zero, via the second output, if the Select input is a second value;

f) a first exclusive-or operator having two inputs and an output, the first exclusive-or operator configured to receive the Left Half input and the Key input;

g) a second exclusive-or operator having two inputs and an output, the second exclusive-or operator configured to receive the result output via the second output of the first group of transistors and the output of the first exclusive-or operator; and

h) a third exclusive-or operator having two inputs and an output, the third exclusive-or operator configured to receive the result output via the first output of the first group of transistors and the Left Half input.

17. (Currently amended) The execution unit of ~~claim 15~~ claim 16, further comprising a second group of transistors configured to receive data output by the second exclusive-or operator.

18. (Currently amended) The execution unit of ~~claim 15~~ claim 16, wherein the execution unit is operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or an OFB mode of DES encryption at the same time that the first group of transistors performs one or more of the following actions: receiving the table input, performing the table look- up, and outputting data.